WHAT IS CLAIMED IS:

1. A method of manufacturing a pull-up transistor for use with a Vdd terminal and an I/O pad of a semiconductor device comprising:

forming a gate insulating layer in an active region on a first conductive-type semiconductor substrate;

forming an impurity implantation region at a predetermined first sector within the substrate by ion-implanting an impurity of a second conductive-type;

forming a gate on the gate insulating layer over at least a portion of the first sector and over a region adjacent to the first sector;

forming source and drain regions within the substrate at opposite sides of the gate by ion-implanting an impurity of the second conductive type, the first sector having been predetermined such that the impurity implantation region does not reach both the source region and the drain region;

coupling one of the source region and the drain region to the I/O pad; and

coupling the other one of the source region and the drain region to the Vdd terminal.

2. The method of claim 1, wherein the gate is formed by depositing a conductive layer and then selectively etching it.

3. The method of claim 1, wherein forming the impurity implantation region is by ion-implanting at a low concentration.

4. The method of claim 1, further comprising:

forming LDD regions at both sides of the gate; and

forming a spacer adjacent the gate before forming the source and drain regions.

5. A pull-up transistor for use with a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductive-type;

a source region and a drain region of a second conductive type formed in the substrate and defining between them a channel region, one of the source region and the drain region being coupled with the I/O pad, the other one of the source region and the drain region being coupled with the Vdd terminal;

an impurity implantation region of impurities of a second conductive-type formed in a first sector of the channel region, the first sector reaching at most one of the source region and the drain region;

a gate insulating layer on the substrate over at least a portion of the impurity implantation region and over at least a portion of an area adjacent the impurity implantation region; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of a region adjacent to the first sector.

6. The transistor of claim 5, wherein the first sector has a narrower line width than a line width of the gate.

7. The transistor of claim 5, wherein the gate is over a first portion of the first sector and over a second portion of an area adjacent the first sector, and wherein the first portion is in a predetermined ratio with the second portion.

8. The transistor of claim 5, wherein the first sector does not reach either one of the source region and the drain region.

9. The transistor of claim 8, wherein the first sector is separated from the source region and from the drain region by equal distances.